**Reg. No. \_\_\_\_\_\_\_\_**

**Karunya University**

**(Karunya Institute of Technology and Sciences)**

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May-2013**

**Subject Title: VLSI DIGITAL SIGNAL PROCESSING Time: 3 hours**

**Subject Code: 12EC317 Maximum Marks: 100**

**Answer ALL questions (5 x 20 = 100 Marks)**

1. a. With the system diagram explain the LMS adaptive filter.

b. For the DFG shown the computation times of the nodes are shown in the parentheses. Compute the iteration bound of the DFG using

i. Longest Path Matrix algorithm and ii. Minimum Cycle Mean algorithm.



(OR)

2. a. Draw DFG and hence explain the direct-form 3-tap FIR filter and transposed 3-tap FIR

filter.

b. In the SFG shown in the figure, the computation time for each is assumed to be 1 u.t.



Calculate the critical path computation time.

The critical path has been reduced to 2 u.t by inserting 3 extra delay elements as shown in the following figure. Is this a valid pipelining? If not, obtain an appropriate pipelined circuit with critical path of 2 u.t



[P.T.O]

3. Draw a constraint graph and use it to determine if the following system of inequalities has a

solution, and find a solution if one exists using

a. The Bellman-Ford algorithm and b. the Floyd-Warshall algorithm



(OR)

4. a. Retime the DFG to reduce the number of registers while achieving a clock period of 2

u.t. Assume that addition and multiplication requires 1 u.t and 2u.t respectively.



b. Explain the unfolding algorithm.

5. Explain in detail about Life Time analysis.

(OR)

6. Explain in detail about the systolic array design methodology.

7. Discuss in detail about roundoff noise properties in pipelined 1st order and 2nd order direct form IIR filters.

(OR)

8. Explain parallel multiplication with (a) Sign extension and (b) Modified Booth recoding.

9. **Compulsory:**

a. Explain in detail about Wave Pipelining.

b. Explain sub expression sharing in Digital Filters.